Eleventh Quarterly Report
on
Molecular Circuit Development

Contract No. NOw 60-0362-c

Submitted to

U. S. DEPARTMENT OF THE NAVY
BUREAU OF NAVAL WEAPONS
Washington 25, D. C.

MELPAR INC
A SUBSIDIARY OF WESTINGHOUSE AIR BRAKE COMPANY
3000 ARLINGTON BOULEVARD FALLS CHURCH, VIRGINIA

ELEVENTH QUARTERLY REPORT

ON

MOLECULAR CIRCUIT DEVELOPMENT

Period of 15 November 1962 to 15 February 1963

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MELPAR, INC.
3000 Arlington Boulevard
Falls Church, Virginia

ULTIMATE PROGRAM OBJECTIVE

The ultimate objective of this program is to acquire the technical knowledge and capability to provide instruction for the formation of complete thin-film circuits and systems in which electronic circuit elements are integrated in a material matrix to a point where individual elemental appearances have been lost. The circuits will be capable of operating at 500°C, and should possess a high degree of radiation resistance. The circuits, as conceived, will contain microareas within a single film and/or be formed of layers of metals, semiconductors, and dielectrics in preconceived configurations to provide the necessary electronic functions. The objective is to be accomplished by performing studies of film and microcrystal formation, surface and interfacial phenomena, and geometric studies of configurations to use, to the maximum advantage, the physical effects that occur in thin films. The electronic circuits so formed will possess a maximum degree of microminiaturization.

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1. INTRODUCTION

This is the eleventh quarterly report on Molecular Circuit Development submitted in compliance with Contract NOw 60-0362-c. As stated in the Ultimate Program Objective, the purpose of this program is to provide research and development in materials and techniques suitable for formation of molecular circuits. The program is divided into the major areas of materials research and microdevice research.

The phase of the program concerned with pyrolytic deposition of silicon has been completed. The conditions for obtaining either uniform films or crystallites were established. It was found that silicon crystallites of several mils in diameter could be reproducibly obtained, while crystallites of up to 20 mils in diameter could be formed on occasion. The emphasis will be placed on pyrolytic deposition of materials suitable for high-temperature operation.

Studies of germanium films formed in an ultrahigh vacuum chamber have led, within experimental limits, to the conclusion that background pressure during deposition does not have a significant effect on the film properties. These results indicate that further efforts in this direction are not warranted. Sputtered films of silicon carbide of much improved mobilities have been produced. Partial crystallization of silicon carbide films was achieved through high-temperature treatment.

The oxides of neodymium and hafnium are now being investigated for use as high-temperature, thin-film dielectrics. The initial studies have been concerned largely with problems of vacuum evaporation of these refractory materials.

Considerable knowledge has been gained regarding the formation of films of the sulfide and selenide of cadmium by vacuum evaporation; film reproducibility has been considerably improved, although final film properties cannot yet be satisfactorily predicted on the basis of deposition and processing conditions. The better films have allowed fabrication of field effect devices with improved characteristics; values of transconductance as large as 15,000 μ-mhos have been measured. A study of the thermal stability of the devices has been initiated. A number of these devices have been used in several operating test circuits to gain familiarity with the operating parameters. The field effect device has also been the object of a theoretical study based on parameters which are analogous to those utilized for description of thermionic vacuum tubes.

The aspect of microdevice research concerned with development of junction devices will shift in emphasis from silicon to higher-temperature materials, such as silicon carbide. The considerable experience gained in the diode and junction develpment, in both germanium and silicon, will furnish the background for this new phase.

2. MATERIALS RESEARCH

Several phases of the materials research program have been completed during the past quarter. Pyrolytic deposition of both crystallites and films of silicon is regarded as adequately developed, and has now been terminated. Attention will be given to the pyrolytic deposition of high-temperature materials, particularly silicon carbide.

Evaporation of germanium under conditions of ultrahigh vacuum was carried out, but, because no clear advantages were found for the technique, this effort will not be continued. Vacuum evaporation of other semiconductive materials has been limited to the II-VI compounds, particularly cadmium sulfide and cadmium selenide, those materials which had proved to be most useful for the field effect devices. Considerable improvement in the sputtered silicon carbide films has been realized; this is attributed to the use of a source material with lower levels of contamination.

Investigations of high-temperature dielectric films have been extended to the oxides of neodymium and hafnium. These refractory materials show considerable promise, although difficulties with the deposition techniques remain to be overcome.

2.1 Pyrolytic Deposition of Semiconductive Films

During this quarter, investigations of the pyrolytic deposition of silicon through hydrogen reduction of $SiCl_4$ were completed. The recent effort has been directed toward reproducibly depositing large crystallites of silicon on fused silica substrates, and toward investigating the electronic

behavior of the crystals and large-area films. Reproducible production of large-crystal silicon was accomplished in the apparatus described previously (See Ninth Quarterly Report, pages 11-15, and figure 3), with the further modification that the nozzle-to-substrate distance was increased to a maximum of three inches. It appears, from the success obtained with this modification, that aerodynamic factors play a major role in the nature of the silicon deposit obtained. The crystals that were grown this period were used for fabrication of experimental diodes. The films of polycrystalline silicon were evaluated for electronic behavior; those films which were not too high in resistance for Hall mobility measurements showed no Hall effect. Inspection of the films by low-magnification microscopy revealed cracks in the films, resulting from the wide difference in coefficients of thermal expansion of the silica substrates and the silicon films.

Because of the termination of work on pyrolytic deposition of silicon, a brief review of relevant observations is given in the following paragraphs.

At substrate temperatures above 1150^{o}C, $SiCl_4$ concentrations between 0.50 and 0.75 percent, and linear gas velocities between 15 and 17 cm-sec^{-1} (STP), large crystals were preferentially grown to a size between 5 and 10 mil diameter. To achieve this crystal growth reproducibly, the nozzle-to-substrate distance must be greater than 2.5 inches and the plane of the substrate must be no greater than 45^{o} from the axis of flow.

To produce compact, uniform silicon films reproducibly, substrate temperatures of 1050-1100°C, linear gas velocities between 17 and 21 cm-sec^{-1}, and a $SiCl_4$ concentration of about 1 percent are needed. Positioning of the substrate perpendicular to the direction of gas flow is conducive to film growth.

Nonadherent, yellow, "amorphous" silicon was formed at substrate temperatures below 1000°C. This low-temperature deposit was shown by X-ray diffraction and chemical analysis to be exclusively silicon and not a $(SiCl_2)_n$ polymer, as suggested in the literature.

The preference for deposition of crystallites or films was not affected by either hydrogen partial pressure or total pressure. Therefore, operation at one atmosphere of hydrogen is recommended, regardless of the type of deposit desired. However, it was observed that the overall growth rate of silicon deposit is affected by hydrogen partial pressure in a nonlinear manner for all types of silicon deposits.

Finally, crystallites and films were successfully deposited on a number of substrates, including fused silica, tantalum (predeposited on silica), and molybdenum. With molybdenum substrates, however, there were indications that a large portion of the silicon reacted to form $MoSi_2$.

At present, the deposition apparatus previously used for silicon is being prepared for the studies of silicon carbide deposition by pyrolysis, or reduction of tetraethylsilane and by reduction of a mixture of $SiCl_4$ and CCl_4. The investigations of pyrolytic film formation will now be directed toward such high-temperature materials.

2.2 Ultrahigh Vacuum Deposition of Germanium

Several germanium films were deposited under vacua as low as 10^{-8} Torr to investigate the effect of background pressure during formation on the properties of the films. The films were formed in an ion-pumped chamber which had previously been used for contact potential studies (See Second Quarterly Report). The chamber was baked at 250-300°C for some time and then cooled to room temperature, normally reaching an ultimate pressure in the low 10^{-9} or high 10^{-10} Torr region before deposition of films. The pressure rise during deposition was found to result primarily from source outgassing, which depended strongly on the type of source used for the deposition. The use of a carbon crucible was observed to be the least satisfactory of the sources used in this respect. A tantalum boat was the most satisfactory.

Using n-type germanium source material, eight films were deposited at rapid evaporation rates onto Code 1723 glass substrates held at 450-550°C, at pressures down to 10^{-8} Torr. Film properties are given in table I. Film thicknesses ranged from 0.13 to 2.8 microns, and resistivities from 0.05 to 0.2 ohm-cm. All films were p-type. The mobilities observed (22-41 cm^2/volt-sec) agreed for the most part with data accumulated for many films evaporated in the 10^{-5} Torr region for the same substrate temperatures and film thicknesses. The films were also checked for field effect, the magnitude of which was comparable with that of films formed under similar conditions at 10^{-5} Torr. Film properties of interest are apparently insensitive to decreases in ambient pressure during

Table I

Properties of Ultrahigh Vacuum Evaporated Germanium Films

Sample No.	Substrate temp (^{o}C)	Thickness (microns)	R_{DC} (ohms)	Resistivity (ohm-cm)	Hall coefficient (cm^3/coul)	Hall mobility (cm^2/volt-sec)	Hall mobility of comparable films formed at 10^{-5} Torr (cm^2/volt-sec)
UGe 1	450	0.134	40K	.249	7.8	31	5-30
2	do.	.134	16K	.093	1.6	12	5-30
3	do.	.589	3K	.071	1.7	22	20-60
4	do.	.200	9K	.057	2.4	41	10-40
5	do.	.51	3.5K	.066	2.3	35	20-60
6	do.	.402	3.5K	.057	2.1	38	10-50
7	do.	2.8	980.	.15	4.6	31	130-150
8	550	.214	6K	.056	1.8	31	10-40

evaporation of up to a thousandfcld. Because of this independence, deposition of germanium films under conditions of ultrahigh vacuum will not be pursued further.

2.2.1 Deposition of II-VI Compounds

Vacuum deposition of other materials has been concerned with cadmium sulfide and cadmium selenide this quarter. Considerable improvement in film properties has been realized with these materials through a number of modifications made in the deposition procedures. Among the refinements made were the following:

a. Redesign and rearrangement of the substrate heater to ensure greater uniformity of the substrate temperature.

b. Shielding of boat-electrode contacts with tantalum sheet to minimize the possibility of film contamination caused by copper.

c. Reduction in the number of substrates on which films are deposited per run from nine to four to ensure more uniform deposition.

d. More frequent and thorough cleaning of the vacuum system.

The properties of some of the cadmium selenide films are given in table II. All of these films were deposited at low substrate temperatures. Some general observations, from these and other results, are:

a. Film resistivity increases with
   (1) Increased substrate temperature during deposition,
   (2) Decreasing rate of evaporation,
   (3) Increased annealing time and temperature,
   (4) Decreasing film thickness.

Table II

Properties of Evaporated CdSe Films

Sample No.	Deposition pressures (Torr)		Substrate temp (°C)		Thickness (Å)	Resistivity (ohm-cm)	Anneal temp (1) (°C)	Hall mobility (cm^2/v-sec)	DC Resistance (Kohms)
	Begin	End	Begin	End					
1	$7x10^{-6}$	$1x10^{-5}$	-30	-10	7050	1.59	200	50	140
2	$1x10^{-5}$	$3x10^{-6}$	-13	+10	3740	78.5	200	--	8000
3	$5x10^{-6}$	$2x10^{-5}$	+10	+30	2940	.0258	200	54.5	2.5
4	$2x10^{-5}$	$2x10^{-5}$	+31	+53	--	∞	200	--	∞
5	$2x10^{-5}$	$3x10^{-5}$	+60	+65	5350	.0752	200	9.5	3.4
6	$3.5x10^{-5}$	$3.5x10^{-5}$	-8	+13	4330	.0775	200	53	7.0
7	$2.8x10^{-5}$	$1.3x10^{-6}$	-10	+36	6690	2.81	200	--	120
8	$4x10^{-5}$	$2.8x10^{-5}$	+31	+67	1220	.0172	200	3.9	42
9	$1.4x10^{-5}$	$2.2x10^{-5}$	+58	+64	790	.285	200	15.7	74
10	$3x10^{-4}$	$2x10^{-5}$	-2	+23	--	∞	200	--	∞
11	$1.2x10^{-5}$	$2x10^{-6}$	-20	+3	2680	1.59	200	40	100
22	$1.8x10^{-5}$	$2.3x10^{-4}$	+30	+54	7000	0.57	300	37	20
26	$2x10^{-5}$	$3.2x10^{-4}$	+35	+57	5350	.047	75	19.6	2

(1) For period of 10 minutes.

b. Films prepared from highly purified, undoped CdSe, as well as CdS and CdTe, have always been found to be n-type.

c. Films are considerably less light sensitive when annealed in vacuo and immediately overlaid with a dielectric film.

d. Considerable lowering of film resistivity generally occurs as a subsequent dielectric film is deposited by as much as a thousandfold. This is probably caused by stresses induced in the semiconductor by the dielectric film.

e. Higher mobilities seemed to be favored by increases in the pressure of the system during deposition, but attempts to verify this were inconclusive.

Subsequent to deposition, the films undergo large changes in resistivity during processing steps. Typical behavior of a CdSe film as a function of substrate temperature is shown in figure 1. The active area of this film was 1/400 of a square. The film was deposited on a substrate cooled to -30°C. This was accomplished by the liquid nitrogen cooling of a copper block which served as the substrate holder. Immediately following deposition of the film, a resistance of 5 megohms was measured. As the substrate temperature rose to room temperature, the resistance decreased to 6KΩ. Annealing at 200°C for a period of 10 minutes then caused the resistance to increase to 9.5 KΩ. The film resistance continued to rise to 30KΩ as the substrate temperature was lowered to 100°C. Upon deposition of the SiO dielectric at 100°C, the resistance dropped rapidly to 700 ohms. During cooling to room temperature,

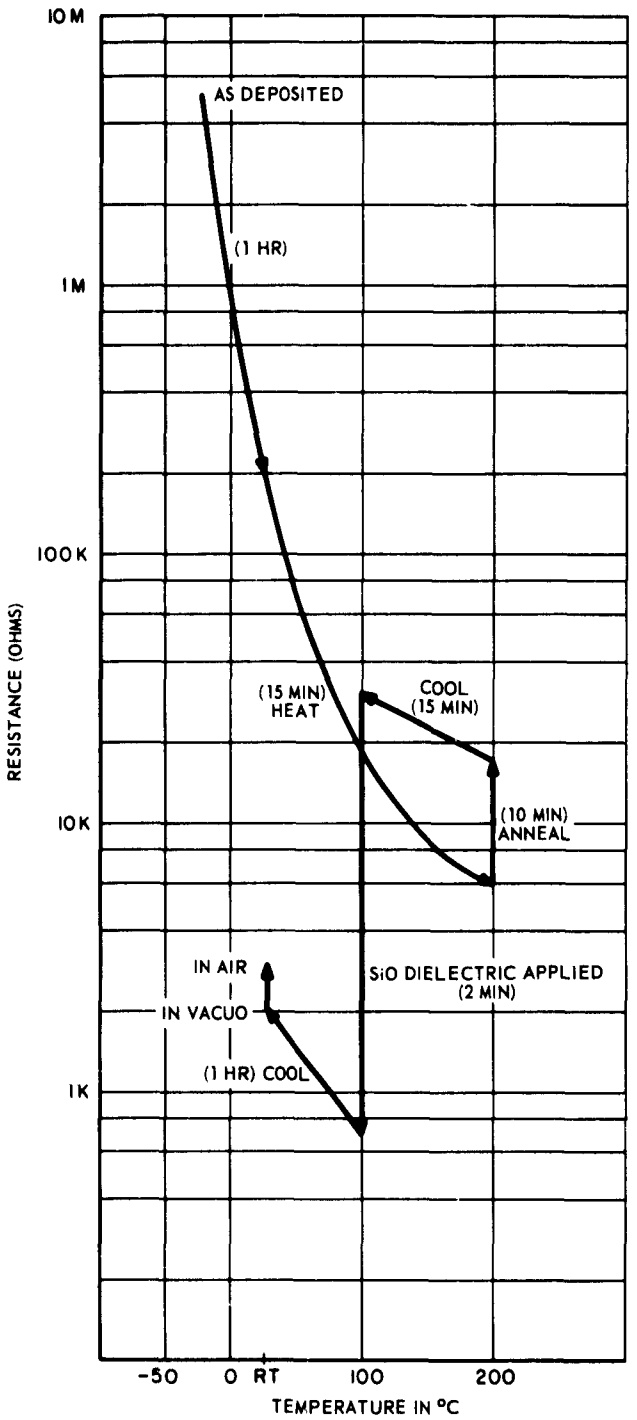

Figure 1. Resistance Behavior of Evaporated CdSe Film During Device Formation

the film resistance agin rose to 2KΩ and a further rise to 2.8 KΩ occurred when the sample was withdrawn from the chamber. These extensive variations point out the difficulty of predicting final film resistance from a knowledge of film thickness and processing conditions.

X-ray fluorescence techniques were used to study cadmium sulfide and selenide films for stoichiometry. Table III shows typical results.

Table III

Stoichiometry of CdS and CdSe Films

Color of Film		
		CdS
Yellow	$\frac{Cd}{S} = \frac{1}{1.023}$	(excess sulfur)
Brown	$\frac{Cd}{S} = \frac{1.022}{1}$	(excess cadmium)
		CdSe
Light Brown	$\frac{Cd}{Se} = \frac{1.1}{1}$	(excess cadmium)
Dark Brown	$\frac{Cd}{Se} = \frac{1}{1.07}$	(excess selenium)

The CdS films which are yellow in appearance are extremely high in resistance; such films occur when formed at substrate temperatures of 200^{o}C or above or annealed at high temperatures. The dark-colored, brown-to-black films of CdS form at low deposition temperatures; the excess of cadmium leads to resistance values which are much too low to be useful in devices. Orange-colored CdS films, which resemble the source material in appearance, are found to be preferable for use in field

effect device fabrication because of the intermediate values of resistivity.

The appearance of CdSe films, on the other hand, may vary from transparent to a dark, reflective brown. The colors, however, are less indicative of film resistivity. The lighter-colored films contain an excess of cadmium and are generally quite low in resistance; they are usually formed at low substrate temperatures and at slow rates of deposition. Dark brown, reflective CdSe films generally result from fast rates of deposition or substrate temperatures above 50°C; the resistivity values of these films are quite sensitive to the annealing procedure. However, generalizations concerning relationships between appearance of a film and its usefulness for field effect devices cannot yet be stated for the selenide.

2.3 Sputtered Semiconductive Films

The recent emphasis in work on film formation by means of cathodic sputtering has been centered on silicon carbide, continuing the program initiated during the previous quarter. Some of the recent results are quite encouraging.

2.3.1 Experimental

Silicon carbide films have been sputtered from sources furnished by two different suppliers. The "KT" grade, self-bonded material of the Carborundum Co., described in the last quarterly report, was used as source for samples through S-SiC 17 in the accompanying table. This source is in the form of a thin, rectangular slice. Significant levels of contamination due to Al, Cr, Cu, Fe, Mn, Ni, Ti, and V, as well as traces of several other elements, were found by means

of arc spectrographic analysis of this material. Most of the film samples deposited from this source were in the form of the small, 4-sample field effect pattern.

A silicon carbide source of greater purity was procured from the Exolon Co. This material is in the form of a mass of clustered crystallites so that the sample source presents many, more or less randomly oriented, crystalline facets to the bombarding gas ions. Arc spectroscopy indicated for this material a fairly high impurity level of aluminum, as well as traces of Cu, Fe, Mg, V, and Ti. Samples S-SiC 18 through 25 were formed from this material.

Several of the SiC films have been treated thermally at temperatures up to 1200^{o}C in atmospheres of argon. Preliminary measurement runs of resistance vs. temperature were also performed for two of the films to determine thermal band gaps.

Several attempts at obtaining information about the films from infrared reflectance spectra have been made with the hope that this technique would serve to characterize these films, which appear amorphous to X-ray diffraction. The spectra were ambiguous, however, probably as a result of interference caused by the fused silica substrate.

2.3.2 Results

Data on the SiC films sputtered during this quarter are presented in table IV. Notable differences between samples prepared from the two sources are evident, particularly with regard to the Hall mobilities. S-SiC 12 is n-type, with a Hall mobility of 0.5 cm^{2}/v-sec, while S-SiC 22 and 23 are p-type, with respective mobilities of about 17 and 15; lower values of resistivity are also found for the later samples.

Table IV

Properties of Sputtered SiC Films

Sample No.*	Substrate material	Deposition temp (°C)	Argon pressure (μ)	Potential (KV)	Sputtering time (hrs)	Anneal conditions	Film thickness
S-SiC 12	Fused SiO_2	740-770	170	4.2-4.5	1-1/4	730°/1/4 hr	3500
14**	do.	650	50	3.7	3/4	650°/1/3 hr	200 to 80C
15**	do.	660	120	3.9-4.1	3/4	650°/1/3 hr	~1300
16**	do.	720	50-150	4.5-4.9	5/6	700°/1/4 hr	300 to 300
17**	do.	560	100	3.9	3/4	560°/3/4 hr	~4000
18	Al_2O_3	400	90	3.6	1	400°/1/3 hr	~2500
19	do.	450	70	4.2	1-1/4	None	~3500
20	SiO_2	440	50	3.9	1-1/2	440°/1/4 hr	2000
21	do.	700	75	3.4	1-1/3	None	2100
22	do.	~700	90	3.8	1-2/3	650°/1/4 hr	2100
23	Al_2O_3	750	110	3.2	1-1/2	720°/1/4 hr	~2700
24	do.	500	90	2.9-3.1	1-1/3	500°/1/4 hr	~3000
25	do	375	70	3.5	1-1/4	375°/1/4 hr	(thin)

* Samples S-SiC 12 through 17 formed from Carborundum Co. source material; samples 18 through 2

** Field effect samples; resistivities estimated from probe resistance values.

Table IV

Properties of Sputtered SiC Films

Sputtering time (hrs)	Anneal conditions	Film thickness (Å)	Apparent resistivity (Ω-cm)	Carrier type	Hall mobility (cm^2/v-sec)	Appearance of film
1-1/4	730°/1/4 hr	3500	0.013	n	0.5	metallic, brown-black
3/4	650°/1/3 hr	200 to 800	(0.02)	-	-	metallic, gray-black
3/4	650°/1/3 hr	~1300	(0.3 to 1.3)	-	-	metallic, gray
5/6	700°/1/4 hr	300 to 3000	(0.6 to 1.4)	-	-	metallic, gray-black
3/4	560°/3/4 hr	~4000	(0.8 to 10)	-	-	gray-green
1	400°/1/3 hr	~2500	∞	-	-	yellowish
1-1/4	None	~3500	∞	-	-	brownish
1-1/2	440°/1/4 hr	2000	∞	-	-	transparent
1-1/3	None	2100	(>10^9Ω)	-	-	transparent, brownish
1-2/3	650°/1/4 hr	2100	0.0017	p	17.4	metallic
1-1/2	720°/1/4 hr	~2700	0.002	p	14.6	metallic, gray
1-1/3	500°/1/4 hr	~3000	∞	-	-	brownish
1-1/4	375°/1/4 hr	(thin)	∞	-	-	yellowish

, source material; samples 18 through 25 formed from Exolon Co. material.

ɔe resistance values.

2

The colors of the films from the two sources show the same effect of substrate temperature. At low temperatures, the films are yellowish and clear, but at higher temperatures they become metallic, gray-to-black in color. This dark color seems to be associated with measurable values of the resistance. Films formed from the Exolon Co. material have been much more uniform in appearance than the earlier films were.

In no case, has an X-ray diffraction pattern been observed for the SiC films as deposited. Sample S-SiC 10 (See 10th Quarterly Report) was treated at 1000°C for 1 1/2 hours and, although resistance decreased considerably, no XRD pattern developed. Samples S-SiC 5 and 6 were also heat treated, at about 1200° for 4 1/2 hours; in both cases, resistance became very high, but, for S-SiC 6, a strong peak corresponding to the principal diffraction line of either α- or β-SiC was developed. For all three of these films, there were indications of some crystallization, but considerable crazing also occurred, undoubtedly because of thermal expansion mismatch of the films and fused silica substrates. Several of the recent films have been deposited on polished alumina substrates to prevent crazing in thermal treatments which are to be carried out later.

The attempts to measure thermal band gaps of SiC films did not give good results. Samples S-SiC 10 and 12 were carried through temperature cyclings to about 700° and 650°C, respectively, while measuring resitance. Calculations of band gap from the measured data give values of the order of 0.1 to 0.2 ev, far below the expected value of 2.8 ev.[1] It

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1. N. B. Hannay, ed., Semiconductors, Reinhold Publishing Corp., New York (1959), p. 52.

is apparent that measurements were not taken to high enough temperatures to enter the intrinsic conduction range. Some lack of agreement between measurements for rising and falling temperatures also indicates that better temperature stabilization during resistance measurements would give improved results.

None of the samples tested gave any indication of a measurable field effect. The samples were formed from both sources, but there had been no attempts to crystallize the films through thermal treatment.

The important conclusions from this work are as follows:

a. Use of the new source of silicon carbide, in the form of clustered crystallites, has given films of much improved uniformity. The films with measurable Hall properties are p-type, and the mobility has been as high as 17 $cm^2/v\text{-}sec$.

b. As observed with the older source material, measurable values of resistance are associated with metallic-appearing films, which are generally gray-to-black in color. Such films are normally produced at temperatures of about $700^{\circ}C$ and above.

c. Development of a definite X-ray diffraction pattern by thermal treatment at $1200^{\circ}C$ indicates that the films can be crystallized. It is expected that this could be more readily accomplished at much higher temperatures.

2.4 Vacuum Deposition of Dielectric Films

Techniques for depositing some of the higher-temperature oxides were studied this quarter to supplement those materials studied previously. A review of the properties of a number of dielectric materials that might be suitable for high-temperature applications is presented in table V. Some physical properties of the bulk forms, as well as the films, are listed for

Table V

Physical Properties of Dielectric Materials Suitable for High-Temperature Applications[1]

Dielectric	Melting point (°C)	Dielectric constant (K)	Index of refraction	Resistivity (ohm-cm)	Crystal structure
TiO_2 (Rutile)	1640 (D)	85-90 (ave.)	2.6^{O} 2.9^{E}	-	Tetragonal
SiO_2 (Vitreous)	(1710)[3]	4.5*F 4.3 (ave.)	1.46*F 1.55 (ave.)	-	Amcrphous
Nd_2O_3	1800	9.8*F	1.71*F	-	Hexagonal
AlN^W	1800 (D)	-	2.2	10^{12} (RT)	Hexagonal
				10^{8} (730°C)	Hexagonal
Si_3N_4	1900 (S)	13 F[2] 4.2*F	-	10^{12} (RT)	Hexagonal
Al_2O_3	2040	10.6 (C-Axis) 8.6(C-Axis) 6.4*F	1.63*F 1.76 (ave.)	10^{11} (500°C)	Hexagonal
La_2O_3	2350	6.7-10-5*F	-	-	Hexagonal
BeO	2570	5.8	-	10^{16} (RT) 10^{12} (1200°C)	Hexagonal
BN	2730 (S)	4.2	1.74	$2x10^{13}$ (RT) $3x10^{4}$ (1000°C)	Hexagonal
HfO_2	2790	3.5*F	2.112*F	-	Monoclinic
CeO_2	2600[4]	3.9*F	-	-	Cubic

Table V (Continued)

1. Bulk information taken from Ceramic Industry (Jan. 1962).
2. C.R. Barns and C.R. Geesner, J. Electrochem. Soc. 107, 98 (1960).
3. Melting point of crystalline silica.
4. Tabulated in N.V. Sidgwick, Chemical Elements and Their Compounds, Oxford Univ. Press (1950), p. 635.

* - Evaluated at this laboratory.
F - Film form.
W - Reactive with water.
D - Decomposes.
S - Sublimes.
O - Ordinary index.
E - Extraordinary index.

comparison. Some dielectrics in this group, such as ceric oxide and hafnium oxide, have extremely high melting points, while others, e.g., lanthanum oxide and neodynium oxide, melt near 2000°C. For materials with melting points below 2200°C, the boron nitride liner/carbon crucible source heater proved to be quite efficient.* Beyond this limit, however, use of this type of source becomes impracticable. Although some work with boron nitride liners has been done up to 2800°C, generally only the liners of highest purity boron nitride can survive a complete film deposition. With this manner of heating the higher-temperature materials, it is generally difficult to obtain films greater than 1000Å in thickness. Thus, it has become necessary to employ other means of heating these refractory oxides. Flash evaporation of ceric oxide from a tungsten boat has produced colorless films, while the same technique has formed hafnium oxide films which were highly reduced.

Hafnium oxide was successfully deposited by heating the material, compressed into pellet form, with an electron beam (current of 50-75 ma at 4 KV). Clear films were formed and X-ray diffraction patterns showed them to be crystalline HfO_2. A typical X-ray diffraction pattern is shown in figure 2. The index of refraction of the same sample was found to be 2.112. The film thickness was 2650Å. Capacitors have not yet been fabricated for determination of the temperature-capacitance characteristics.

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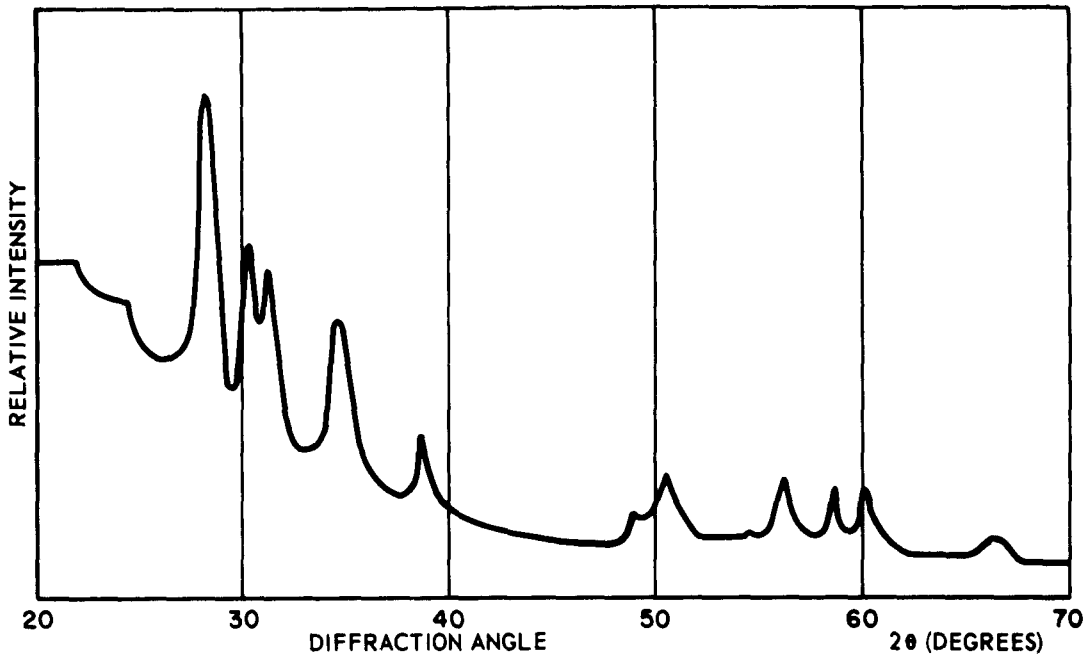
* See Sixth and Seventh Quarterly Reports on Molecular Circuit Development (1961) for a description of this source.



EXPERIMENTAL RESULTS			X-RAY POWDER DATA*	
ANGLE (2θ)	d VALUES	I/I_1	d VALUES	I/I_1
DEGREES	A°	%	A°	%
28.2	3.162	100	3.15	100
30.3	2.947	57	NOT IDENTIFIED	
31.4	2.846	51	2.82	100
34.6	2.590	54	2.59	60
38.7	2.325	21	2.32	50
50.2	1.816	24	1.807	60
56.2	1.635	25	1.634	40
58.4	1.579	24	1.580	30
60.0	1.540	25	1.533	50

*AMERICAN SOCIETY FOR TESTING MATERIALS, SPECIAL TECHNICAL PUBLICATION 48-L(1962); INDEX CARD NO. 6-0318.

Figure 2. X-ray Diffraction Pattern of Vacuum Deposited HfO_2 Film

Neodymium oxide has been deposited from a boron nitride liner and from boats of tungsten and tantalum. Those films deposited from the boron nitride liner were pinhole-free and had low dielectric loss. Capacitors formed when the material was deposited from the metal boats exhibited pinholes. This is caused by spitting of the Nd_2O_3 during deposition, causing localized hot zones, which produce pinholes in the film. The dielectric constant was found to be 9.8 and the index of refraction is 1.711. The temperature coefficient of capacitance and crystalline structure of the films have not yet been investigated.

The ceric oxide films deposited from a tungsten boat were transparent, while the films made by deposition from the BN liner had a slightly straw color. The discolored film changed in capacitance by 10% on being heated to about 490°C.[2] The clear film should exhibit better high-temperature characteristics; it will be investigated accordingly.

The difficulties encountered when attempting to deposit high-temperature oxides have slowed the rate of progress on the oxides. The technique of electron beam heating has not yet been refined sufficiently to make reliable capacitors. The success in the initial film formation studies of the HfO_2 and Nd_2O_3, however, indicates that these materials may prove to be suitable high-temperature dielectrics; they are to be studied more fully.

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2. C. Feldman and M. Hacskaylo, Rev. Sci. Instr. 33, 1459 (1962).

3. MICRODEVICE RESEARCH

The refinements in evaporation techniques for the II-VI compounds have led to improvements in the thin-film field effect device characteristics. With certain configurations, it has been possible to obtain higher values of the transconductance than had previously been attainable. Initial studies have indicated a considerable temperature sensitivity for these devices, although this is recognized as a limitation of the dielectric in part.

A theoretical analysis of operating characteristics of the field effect device has been made. It is expected that conclusions based on this treatment will result in design of devices with improved performance. To evaluate their operation, several circuit incorporating field effect devices were devised and tested.

Development of silicon junction devices is being brought to a close. A summary of developments made under this program, as well as in the prior work with germanium, is included in the discussion. Investigations on junction devices will now be concerned with such high-temperature materials as silicon carbide.

3.1 Thin Film Field Effect Devices

3.1.1 Field Effect Device Characteristics

Continued improvement in the field effect devices was realized this quarter. The devices have become more reproducible as improved deposition techniques are being developed. These techniques have been discussed in paragraph 2.2.1.

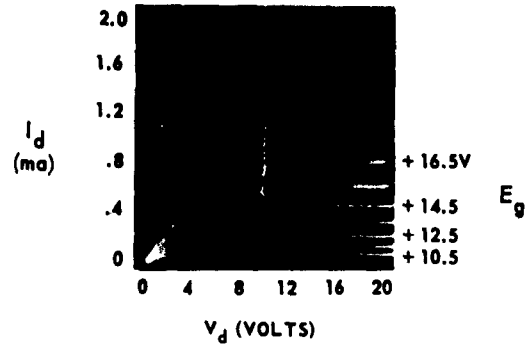
CdSe and CdS devices were concentrated upon this quarter with the aim of improving μ and g_m while reducing the drain resistance. Although voltage gain has been observed in devices utilizing CdTe, as reported last quarter, their study has been set aside temporarily because initial results had been less encouraging in the area of reproducibility.

Figure 3 shows typical improved characteristics for the CdS devices (compare figure 14 of the 10th Quarterly Report). The loops observed in the I_d vs. V_d parameters are as yet not completely understood, but is is recognized that leakage, surface states, and temperature are all important.

Figures 4 and 5 show characteristics of CdSe devices operating in the enrichment and depletion modes, and indicate the general improvement over devices deposited during the last quarter. (See figures 15 and 18 of the 10th Quarterly Report). Transconductance figures as large as 15,000 μ-mhos have been obtained for larger CdSe units, i.e., a source-drain width of 300 mils and an active region width of 0.3 mil. At the present time, however, a source-drain width of 100 mils and an active region width of 0.5 mil are generally employed in these evaluation studies and device characteristics shown.

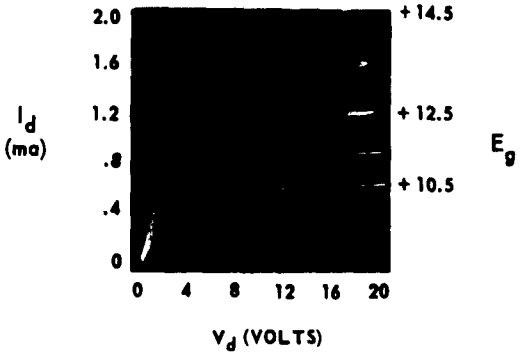
Several thin film field effect devices have been examined this quarter to determine their stability with temperature. Argon, dried over P_2O_5 and passed over heated copper turnings to remove traces of oxygen, was preheated and directed over the device, which is held in a heated "Pyrex" glass sample chamber. The sample temperature was monitored by means of a chromel-alumel thermocouple in contact with the surface of the substrate. Device characteristics, I_d-V_d, were displayed on a curve tracer as the device is heated.

(a) DARK



$g_m \approx 160$ μmhos
$r_p \approx 1$ meg
$\mu \approx 160$

(b) LIGHT



$g_m \approx 400$ μmhos
$r_p \approx 500$ K
$\mu \approx 200$

Figure 3. Characteristics of a CdS Field Effect Device Operating in Enrichment Mode in (a) Dark and (b) Normal Room Light

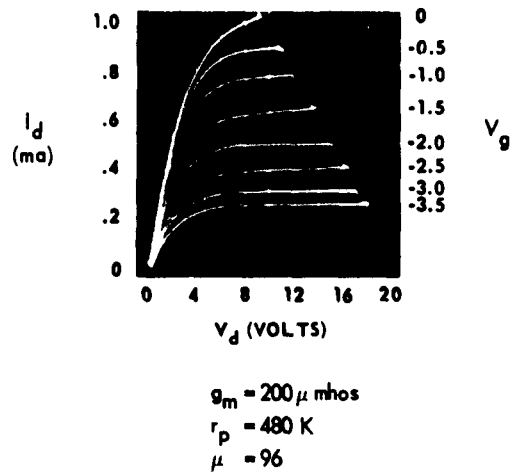


Figure 4. Characteristics of CdSe Field Effect Device Operating in Depletion Mode

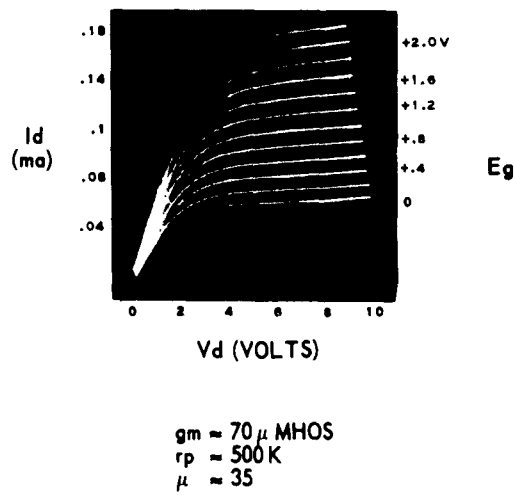


Figure 5. Characteristics of CdSe Field Effect Device Operating in Enrichment Mode

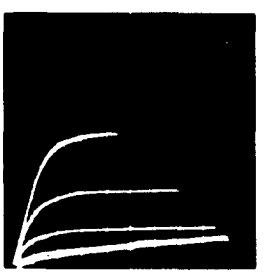
Two devices of cadmium selenide and one of cadmium sulfide have been examined so far. These have all utilized as dielectric silicon monoxide, which, as expected, limited device operation to about 150°C. Between 145° and 165°C, the dielectric failed, resulting in a direct short between gate and semiconductor. Other dielectrics will undoubtedly allow device operation to higher temperatures.

In addition to failure of the dielectric, the source-drain resistance was observed to change with temperature. For example, the initial investigations have shown that the values of resistance of both cadmium sulfide and selenide decrease by a factor of about 30-40 between room temperature and 105°C. To check that this resistance variation is indeed caused by the temperature coefficient of resistance of the semiconductor, lnR was plotted as a function of 1/T. The slopes of the curves obtained with a cadmium sulfide and a cadmium selenide device yielded calculated thermal band gaps of 2.9 ev and 1.4 ev, respectively. These can be compared to values for the bulk of 2.5 ev for the sulfide and 1.7 ev for the selenide. These measured values are sufficiently close to the bulk values that it may be safely inferred that variations in the resistance of the semiconductor are responsible for the behavior described.

Precise measurements of transconductance and voltage gain were not made in these early investigations. Indications, however, were that the values of these parameters change as the sample resistance changes, as would be expected. Detailed measurements will be made next quarter on devices utilizing dielectrics other than silicon monoxide.

Figure 6 (a and b, respectively) shows typical cadmium selenide device characteristics at 71°C, as the device was being heated, and at 72°C, as

71°C, HEATING



72°C, COOLING

VERTICAL SCALE: 0.02 MA/DIV
HORIZONTAL SCALE: 1V/DIV
0.5 VOLTS 1 STEP WITH + 3 VOLTS GATE BIAS

Figure 6. Characteristics of CdSe Field Effect Device at (a) 71°C as device was heated and (b) 72°C as device was cooled

it was being cooled. After being heated, no loops are observed in the curves and saturation characteristics are much more evident. This particular device was heated to a maximum temperature of 147°C over a period of 2-3 hours and returned to room temperature in a similar period. The silicon monoxide dielectric layer shorted at about 66°C as the device was being cooled. The other devices examined this quarter showed, in general, similar changes with temperature.

3.1.2 Field Effect Circuit Characteristics

3.1.2.1 Theoretical Treatment of Operating Devices

Thus far, only partial descriptions of the thin-film field effect device performance have appeared in the literature. The following analysis is intended to describe, at least qualitatively, the device behavior in terms analagous to the well-known vacuum tube parameters, μ, g_m, and r_p. It is anticipated that such an analysis will prove useful for fabrication of devices with improved performance.

It is possible for the device to operate by either one of two basic mechanisms in what are known as the depletion and the enrichment modes. The particular mode of operation is dependent upon the polarity of the transversely applied electric field and the majority carrier type (n or p) of the semiconductor.

Shockley[3] has described the mechanism of operation in the depletion mode, but only for the case of a junction field effect device. His analysis can be extended, with certain modifications, to the operation of the thin-film device in the depletion mode. Operation in the enrichment mode has been treated by Weimer,[4] who makes the limiting assumption that the potential applied to the gate is large when compared with the potential difference between source and drain. The following analysis of the enrichment mechanism considers

3 W. Shockley, Proc. IRE 40, 1365 (1952).
4 P. K. Weimer, Ibid., 50, 1462 (1962).

source-drain voltage variations, which are significant when compared with the gate voltage. This analysis, therefore, has a wider and more practical application than Weimer's does.

Depletion Mode Operation: The treatment given by Shockley for the operation of a junction field effect device can be extended to explain the depletion mode operation of the thin-film device, with an assumed zero surface state density. In the case of the junction device, the applied gate voltage acts directly to reverse-bias the junction and create a depletion layer. In the case of the thin-film device, the applied voltage is distributed between the capacitance across the dielectric and the capacitance across the depletion layer. That is, only a portion of the applied gate voltage acts to establish a depletion layer in the semiconductor.

Consider figure 7, where

C_2 = capacitance formed across the dielectric

C_1 = capacitance of the depletion layer in the semiconductor

V_2 = voltage across C_2

V_1 = voltage across C_1

V_o = applied voltage

To extend Shockley's analysis, we must calculate V_1, the voltage across the depletion layer, or the effective gate voltage, as a function of V_o, the applied gate voltage.

The two capacitances divide the applied voltage, V_o, according to

$$V_1 = \frac{C_2}{C_1+C_2} V_o \qquad (1)$$

where

$$C_1 = \frac{\epsilon_1 A}{X_p}, \quad C_2 = \frac{\epsilon_2 A}{t} \qquad (2)$$

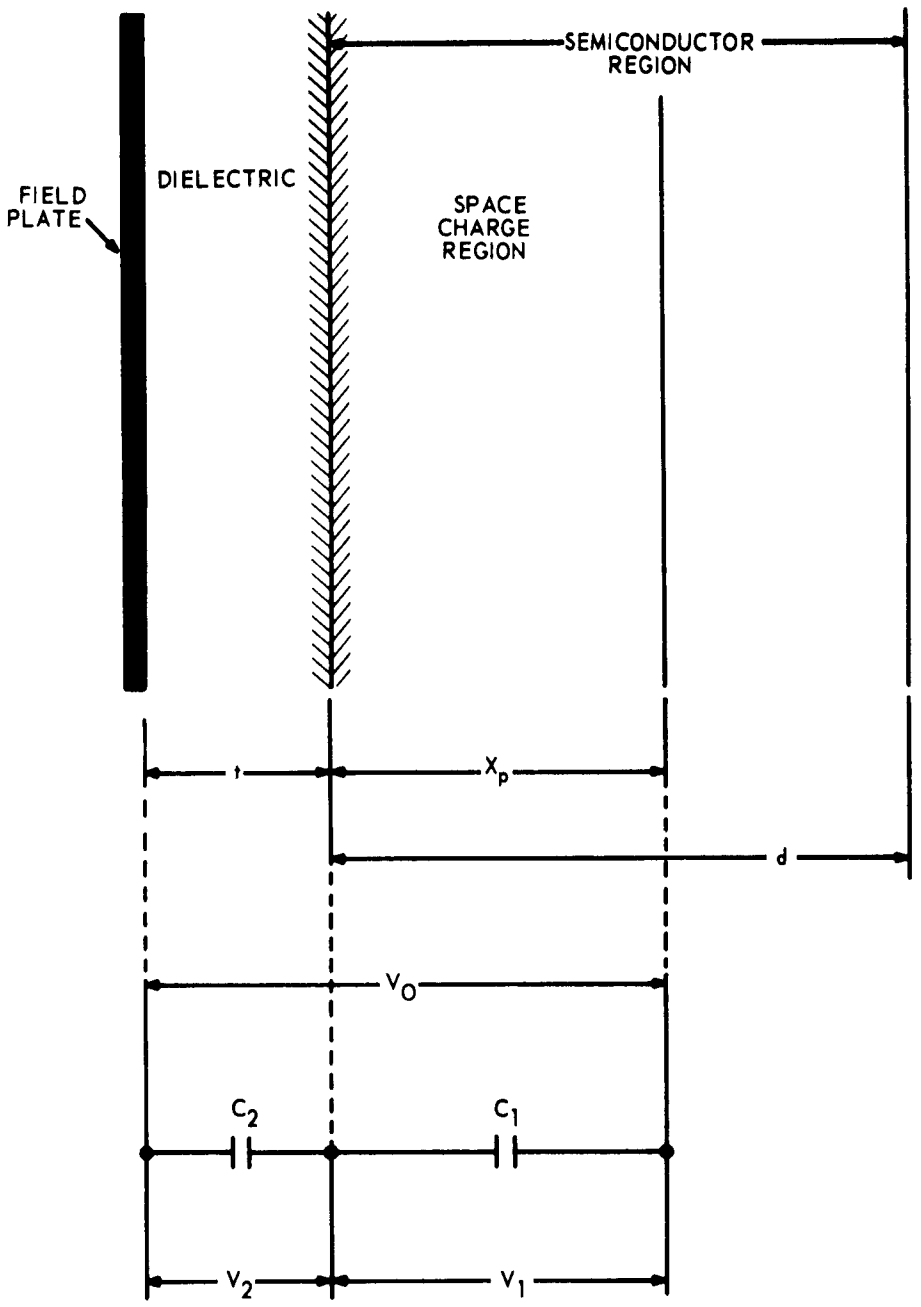


Figure 7. Depletion Mode Operation

A_1 = area of semiconductor exposed to gate

t = dielectric thickness

ε_1 = permittivity of semiconductor

ε_2 = permittivity of dielectric

and X_p is the depth of the depletion layer and is dependent upon V_1 or V_o. This dependence may be arrived at by solving Poisson's equation in the space-charge region of the semiconductor (i.e., $-\frac{\partial^2 V}{\partial x^2} = \frac{\rho}{\varepsilon}$). Under the boundary conditions that the semiconductor is neutral outside the space-charge region, and that the voltage at the dielectric interface is V_1, the solution of Poisson's equation is

$$X_p = \left(\frac{2\ \varepsilon_1 V_1}{qN_a}\right)^{1/2} \tag{3}$$

where q is the electronic charge and N_a is the concentration of acceptors, for a p-type semiconductor (or the concentration of donors for an n-type semiconductor, where N_a is to be replaced by minus N_d.) Implicit in equation 3 is the assumption that all acceptors (or donors) are fully ionized.

Combining equations 1, 2, and 3 yields

$$V_1 = \frac{C_2 V_o}{C_2 + \dfrac{\varepsilon_1 A}{\left(\dfrac{2\varepsilon_1 V_1}{q N_a}\right)^{1/2}}} \tag{4}$$

Solving this quadratic equation for V_1 yields

$$V_1 = \frac{2\varepsilon_1^2 A^2 + 8C_2^2 \left(\frac{\varepsilon_1}{qN_a}\right) V_o - 2\varepsilon_1 A \sqrt{\varepsilon_1^2 A^2 + 8C_2^2 \left(\frac{\varepsilon_1}{qN_a}\right) V_o}}{8C_2^2 \left(\frac{\varepsilon_1}{qN_a}\right)} .$$

The negative sign before the square root is required by the condition that $V_1 = 0$ when $V_o = 0$.

On substituting $C_2 = \frac{\varepsilon_2 A}{t}$ and simplifying the expression for V_1

$$V_1 = \frac{1}{4}\left(\frac{\varepsilon_1}{\varepsilon_2}\right)^2 t^2 \frac{qN_a}{\varepsilon_1} + V_o - \frac{1}{4}\left(\frac{\varepsilon_1}{\varepsilon_2}\right)^2 t^2 \frac{qN_a}{\varepsilon_1} \sqrt{1 + 8\left(\frac{\varepsilon_2}{\varepsilon_1}\right)^2 \frac{\varepsilon_1 V_o}{t^2 qN_a}}$$

or

$$V_1 = K_1 + V_o - K_1 \sqrt{1 + \frac{2V_o}{K_1}} \qquad (5)$$

where

$$K_1 = \frac{1}{4}\left(\frac{\varepsilon_1}{\varepsilon_2}\right)^2 t^2 \frac{qN_a}{\varepsilon_1}$$

Thus, the effective gate voltage (V_1) varies with applied voltage (V_o) according to equation 5, and one may use this relationship to extend the junction analysis of the field effect device to cover the operation of the thin-film device in the depletion mode.

Martin[5], using Shockley's results, obtained the following expression for the drain current of a junction field effect transistor operating

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5 T. B. Martin, Semiconductor Products, 5, 33 (Feb. 1962).

below pinchoff ($V_D - V_G < V_p$):

$$I_D = \frac{1}{R_o}\left\{(V_D-V_G)\left[1-\frac{2}{3}\left(\frac{V_D-V_G}{V_P}\right)^{\frac{1}{2}}\right]-(V_S-V_G)\left[1-\frac{2}{3}\left(\frac{V_S-V_G}{V_p}\right)^{\frac{1}{2}}\right]\right\} \qquad (6)$$

where

V_D = drain voltage

I_D = drain current

V_G = gate voltage

V_S = source voltage

V_P = pinchoff voltage = $(V_D - V_G)$ at pinch off

$$R_o = \left(\frac{\text{length of conductive channel, L}}{\text{conductivity, } \sigma \text{ x area of channel, a}}\right)$$

The transconductance, g_m, of a junction field effect transistor can be calculated from Martin's expression for the drain current. In terms of Martin's parameters, the transconductance is defined by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right)_{V_D}$$

and, in the case of a grounded source configuration, ($V_s = 0$)

$$g_m = \frac{1}{R_o}\left[\left(\frac{V_D-V_G}{V_p}\right)^{\frac{1}{2}} - \left(-\frac{V_G}{V_p}\right)^{\frac{1}{2}}\right] \qquad (7)$$

For the thin-film device, this would correspond to

$$g_m = \left.\frac{\partial I_D}{\partial V_1}\right)_{V_D}$$

This expression, however, does not consider the existance of the capacitance across the dielectric and is, therefore, not a good representation of the thin-film device characteristic. Thus, it is necessary to define a new parameter, g_{mF}, which describes the apparent device transconductance directly in terms of the applied voltage, V_o.

$$g_{mF} = \frac{\partial I_D}{\partial V_D}\bigg)_{V_D} = \left(\frac{\partial I_D}{\partial V_1}\right)\left(\frac{\partial V_1}{\partial V_D}\bigg)_{V_D}\right. \tag{8}$$

Combing equations 5, 7, and 8 yields for the thin-film device (for grounded source, below pinchoff)

$$g_{mF} = \frac{1}{R_o}\left[\left(\frac{V_D - V_G}{}\right)^{\frac{1}{2}}_{V_P} - \left(-\frac{V_G}{V_p}\right)^{\frac{1}{2}}\right]\left[1 - \frac{1}{\left(1+\frac{2V_D}{K_1}\right)^{\frac{1}{2}}}\right] \tag{9}$$

where now $V_G = V_1 = f(V_o)$ and

V_p = the value of $(V_D - V_1)$ at pinchoff = $\frac{\rho d^2}{2\epsilon_1}$

d = thickness of semiconductor

ϵ_1 = permittivity of semiconductor

ρ = charge density

$\rho = N_a$ for p-type materials

$\rho = N_d$ for n-type material

Expressions for the apparent voltage amplification factor, μ_F and the drain resistance r_{df}, may be obtained in a similar manner:*

*The drain resistance, r_{DF}, is analagous to the plate resistance, r_p, of vacuum tube terminology.

$$\mu_F = -\left(\frac{\partial V_D}{\partial V_o}\right)_{S_D} = -\left(\frac{\partial V_D}{\partial V_1}\right)\left(\frac{\partial V_1}{\partial V_o}\right)_{I_D} \tag{10}$$

and

$$= \left\{\left[\left(\frac{V_D - V_G}{V_p}\right)^{\frac{1}{2}} - \left(\frac{-V_G}{V_p}\right)^{\frac{1}{2}}\right] \Big/ \left[1 - \left(\frac{V_D - V_G}{V_p}\right)^{\frac{1}{2}}\right]\right\}\left[1 - \frac{1}{\left(1 + \frac{2V_o}{K_1}\right)^{\frac{1}{2}}}\right]$$

$$r_{d_F} = \left(\frac{\partial V_D}{\partial I_D}\right)_{V_o} = R_o \Big/ \left[1 - \left(\frac{V_D - V_G}{V_p}\right)^{\frac{1}{2}}\right] \tag{11}$$

The expressions above are applicable only for operation before pinch-off, i.e., for $(V_D - V_G) < V_P$. Certain additional assumptions can be made to simplify the analysis in the region near and beyond pinchoff. We may consider the drain current to remain constant beyond pinchoff and equal to the value calculated at pinchoff, i.e., beyond pinchoff we may substitute $\frac{V_D - V_G}{V_P} = 1$ in our previous equations. We may also consider the depletion layer capacitance, C_1, to approach a constant value, $\frac{\epsilon_1 A}{d}$, and to be independent of the applied voltage V_D.

For this case,

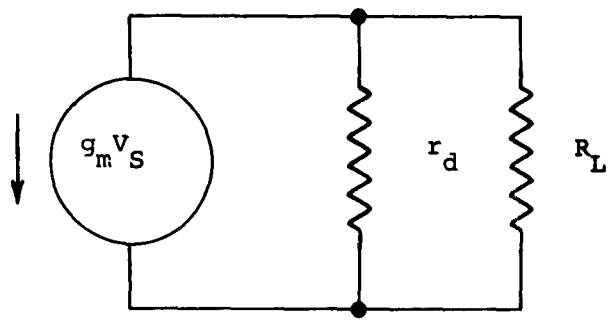
$$V_1 = \frac{C_2}{C_1 + C_2} \; V_o$$

and $$\frac{\partial V_1}{\partial V_o} = \frac{C_2}{C_1 + C_2} = \text{a constant.}$$

The calculation for g_{mF} above pinchoff then yields

$$g_{mF} = \frac{1}{R_o}\left[1 - \left(\frac{-V_G}{V_P}\right)^{1/2}\right]\frac{C_2}{C_1 + C_2} \quad .$$

Obviously, for the assumption of constant drain current, calculations of μ_F and r_{d_F} become meaningless. More sophisticated expressions for operation beyond pinchoff can be obtained by following Shockley's analysis of the "expop" region. Such an analysis is not considered necessary at this point because the expression above for $_{mF}$ is sufficient to describe operation of most present devices. This sufficiency may be illustrated by referring to the elementary circuit analysis of vacuum tube pentodes. The ratio $\frac{r_d}{R_L}$ is usually greater then 10, and sometimes much higher, for present field effect device operation. Thus, for the equivalent circuit shown below,



the output voltage $V_o = g_m V_s \left(\frac{r_d}{r_d + R_L}\right) R_l \approx g_m V_s R_L$

for $\frac{r_d}{R_L} > 10$, with very little error.

Enhancement Mode Operation: The assumptions made in the following analysis for operation of the thin-film device in the enrichment mode parallel those of Weimer, except that the source-drain voltage is recognized to be significant when compared to the applied gate voltage. This recognition extends the range

of application of the results. A zero surface state density will be assumed and, for simplification only, the grounded source configuration will be considered. In addition, only operation by enrichment will be treated, i.e., if an n-type semiconductor is used, V_G, the gate voltage, is assumed to be greater than the potential anywhere within the semiconductor channel. For a p-type material, V_G must be less than the potential anywhere in the channel. Once again, all donors or acceptors, as the case may be, are assumed to be fully ionized.

For the configuration shown in figure 8, the change Δ_Q, that is, induced in the charge in the semiconductor by a changing gate voltage, ΔV_G, and a changing drain voltage, ΔV_D, can be expressed as

$$\Delta Q = \Delta(CV) = C\Delta V + V\Delta C.$$

For enrichment operation, it is assumed that $\Delta C = 0$ (C is capacitance caused by the dielectric only and V is the effective voltage, and, therefore,

$$\Delta Q = C\Delta V.$$

If we assume a linear voltage change through the semiconductor channel, we can express V by an effective voltage change ($V = V_G - V_D/2$). Therefore,

$$\Delta Q = C\ (\Delta V_G - \Delta V_D/2)$$

The drain current I_D can be expressed as

$$I_D = V_D \frac{\sigma \omega h}{L} = V_D \frac{\omega h}{L}(Nq\mu_D)$$

where

σ = conductivity

N = carrier density

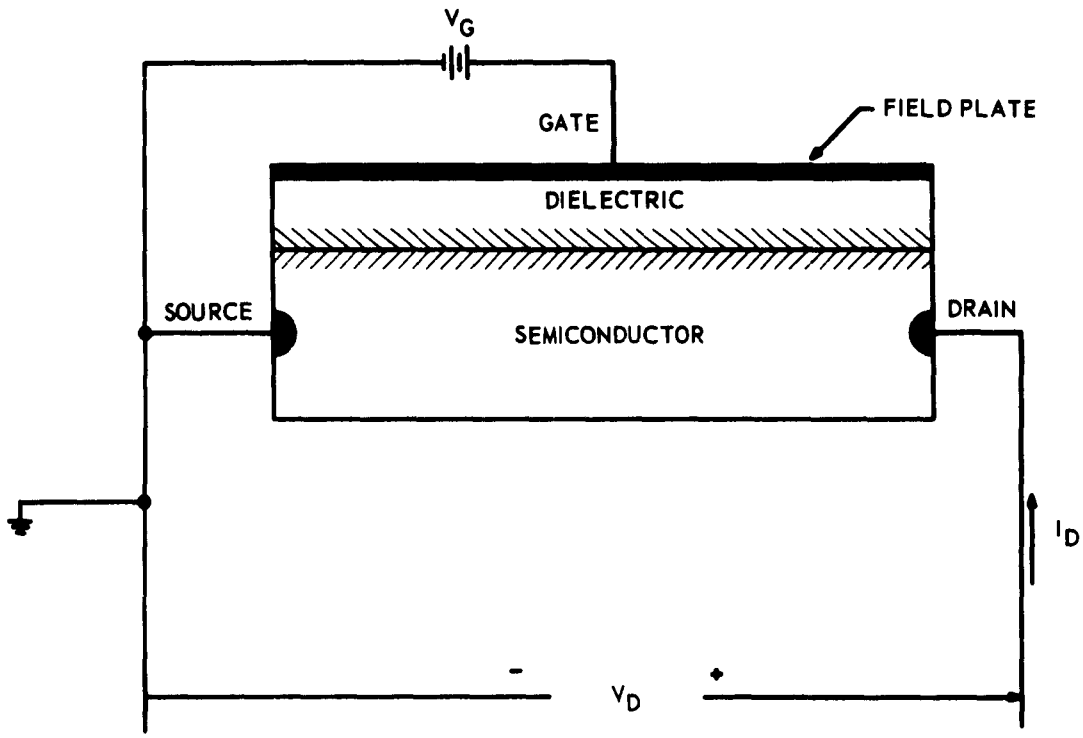


Figure 8. Enrichment Mode Operation

q = electronic charge

μ_D = drift mobility of carriers

ω = width of semiconductor region

h = thickness of semiconductor region

L = length of semiconductor region

Therefore, the change in the drain current is

$$\Delta I_D = \frac{\omega h}{L} (\sigma \Delta V_D + V_D \Delta \sigma)$$

Now the change in conductivity, $\Delta\sigma$, can be approximated by the expression

$$\Delta \sigma = \Delta n q \mu D$$

the substitution of which into the expression for ΔI yields

$$\Delta I_D = \frac{\omega h}{L} q \mu_D (N \Delta V_D + V_D \Delta N) \tag{12}$$

where

$$\Delta n = \frac{\Delta Q}{qL\omega h} = \frac{C \Delta V_G}{qL\omega h} - \frac{C \Delta V_D}{2qL\omega h} \tag{13}$$

For the case under consideration, g_m is defined by

$$g_m = \left.\frac{\Delta I_D}{\Delta V_G}\right)_{V_D} \tag{14}$$

and combination of the three equations above yields for g_m

$$g_m = \frac{\mu_D V_D C}{L^2} , \tag{15}$$

which is an expression identical to that of Weimer. This result should be expected since V_D is a constant in the calculation of g_m.

The calculations of μ and r_d proceed along similar lines, but the effect of the changing drain voltage becomes apparent.

$$\mu = -\left.\frac{\Delta V_D}{\Delta V_G}\right)_{I_D} \tag{16}$$

$$r_d = \left.\frac{\Delta V_D}{\Delta I_D}\right)_{V_G} \tag{17}$$

Substitution of equations 12 and 13 into equation 16 yields, after some manipulation,

$$\mu = \left[\frac{CI_D\mu_D}{(\omega h\sigma)^2}\right] \Big/ \left[1 - \frac{CI_D\mu_D}{2(\omega h\sigma)^2}\right] \tag{18}$$

Similarly,

$$r_d = \left[\frac{L}{\omega hq\mu_D}\right] \Big/ \left[N - \frac{V_D C}{2qL\omega h}\right] \tag{19}$$

Consideration should be given to the signs appearing in equations 15, 18, and 19. Actually, these equations apply directly to an n-type semiconductor channel with positive drain voltage. Negatively applied drain voltages would result in the appropriate sign changes in V_D or I_D as they appear. That is, a change in reference direction in figure 8 necessitates an appropriate change in sign. Equation 13 reveals that a positive ΔV corresponds to a positive Δn. This relationship holds only for n-type material. The corresponding expression for p-type material is

$$\Delta n = -\frac{C\Delta V_G}{eL\omega h} + \frac{C\Delta V_D}{2eL\omega h}$$

This yields for a p-type semiconductor and the reference directions shown in figure 8

$$g_m = -\frac{\mu_D V_D C}{L^2} \tag{15'}$$

$$\mu = -\left[\frac{CI_D\mu_D}{(\omega h\sigma)^2}\right] \Big/ \left[1 + \frac{CI_D\mu_D}{2(\omega h\sigma)^2}\right] \tag{18'}$$

$$r_d = \left[\frac{L}{\omega h q \mu_D}\right] \Big/ \left[n + \frac{V_D C}{2qL\omega h}\right] \tag{19'}$$

Therefore, for operation in the enrichment mode, the analysis for a p-type semiconductor with positive drain voltage is identical to that for an n-type semiconductor with negative drain voltage.

Frequency Considerations: Until now, one of the limiting factors of the field effect device has been the fact that it is inherently a low-frequency device. The device gain-bandwidth product can be approximated by the expression

$$G.B. = \frac{g_m}{2\pi C_g}$$

The input capacitance, C_g, for grounded source operation can be approximated by $C_g = G_{GS} + (1 + A_v)\, C_{GD}$, an expression analagous to that for grounded cathode vacuum tube operation,

where

$$A_v = \frac{V_o}{V_s} = \text{voltage gain}$$

C_{GS} = gate-source capacitance

C_{GD} = gate-drain capacitance

It is clear that the effect of C_{GD} in particular must be reduced to extend the useful frequency range of the device.

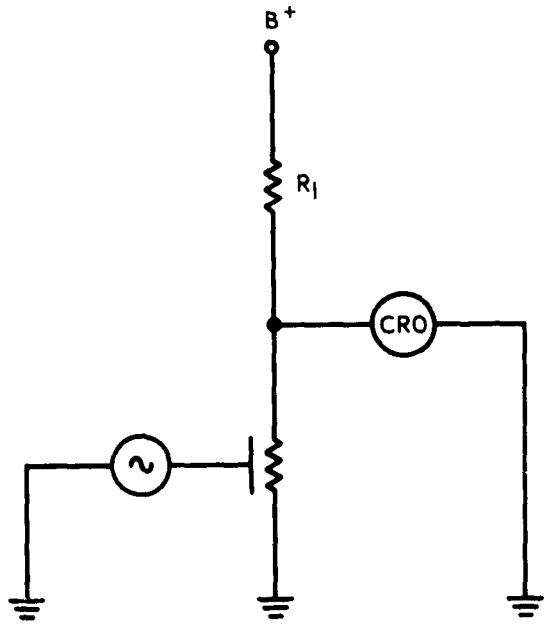
It is suggested that the problem of higher-frequency operation be approached from two general points of view, device design and circuit design considerations. Improved device design should certainly yield the most significant advances initially. Because the gate-drain capacitance is the most serious frequency limitation, it is obvious that modifications to the unit geometry, such as reduction of field plate and semiconductor areas, will directly improve the frequency response. Other geometrical modifications might entail the use of two or even three dimensionally tape red field plates. With the use of such tapered geometries, it should be possible to reduce the gate-drain capacitance without seriously compromising the gain of the device.

The circuit design considerations could include the possible use of various compensating and neutralizing circuits. It is expected that most R.C. coupled vacuum tube techniques for producing high-frequency, wide bandwidth circuits can be modified to extend the frequency utilization of the thin-film field effect device.

3.1.2.2 Prototype Test Circuits

Several thin-film circuits incorporating CdSe field effect devices and rhenium resistors were fabricated this quarter.

Figure 9 shows a schematic diagram for a single-stage amplifier and the input and output waveforms for a device operating in such a circuit.



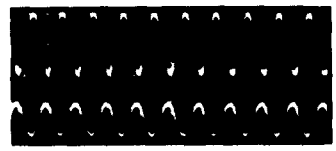


Figure 9. (a) Amplifier Schematic Diagram and (b) Input and Output Waveforms

The input and output signals are 180 degrees out of phase for this particular configuration. The phase relationship between input and output signals is governed by the polarity of the supply voltage and the conductivity type of the semiconductor, and can be arbitrarily put into or out of phase. The amplified signal contains very little distortion.

In figure 10, the output of an oscillator circuit is shown. From the schematic diagram, it can be seen that the first-stage amplifier is coupled directly to the second stage, and the output of this stage is, in turn, fed directly back to the first stage. Sinusoidal oscillations of low distortion have been achieved with such circuits.

The diagram for a free-running multivibrator and the actual output waveform of such a circuit are presented in figure 11. This circuit is similar to that shown in figure 1, but with field effect devices replacing the two load resistors. Operating frequencies from 4 cps to 5000 cps have been observed, with rise times of about 200 microseconds and fall times of about 250 microseconds. For this particular circuit, the frequency and amplitude of the output are sensitive to variations in the supply voltage.

3.2 Junction Devices

Work has continued this quarter on silicon junction devices. The immediate concern has been to produce active devices from silicon crystallites formed in pyrolytic films. This goal has now been achieved. An earlier review of the thermal properties of materials has been brought up to date and certain conclusions drawn regarding those materials which are most suitable.

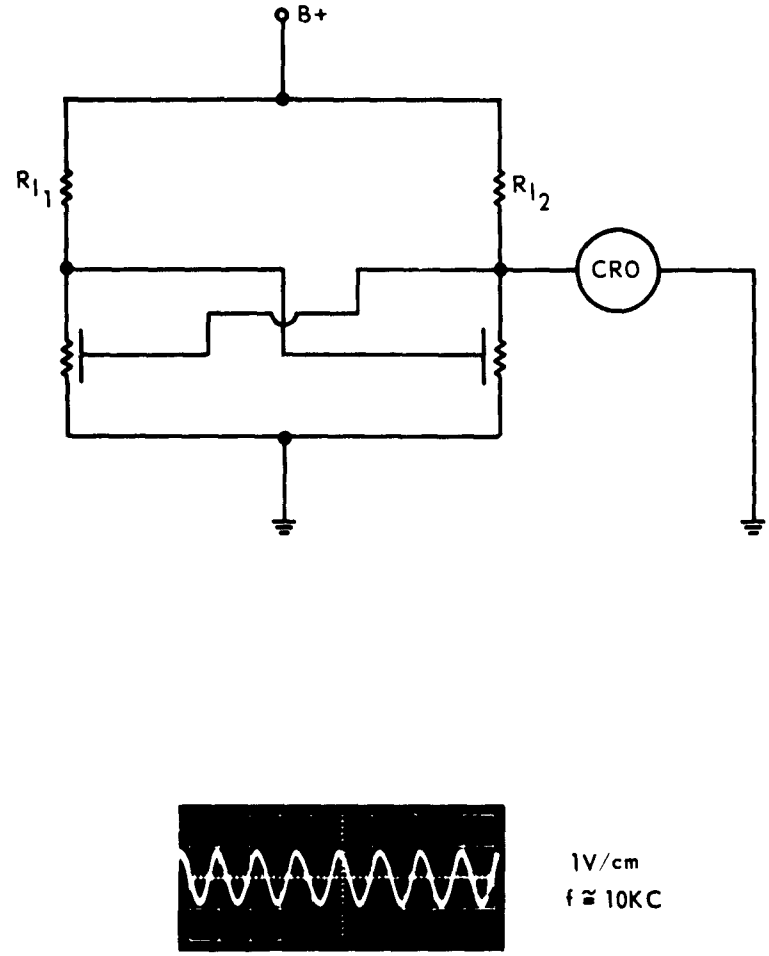
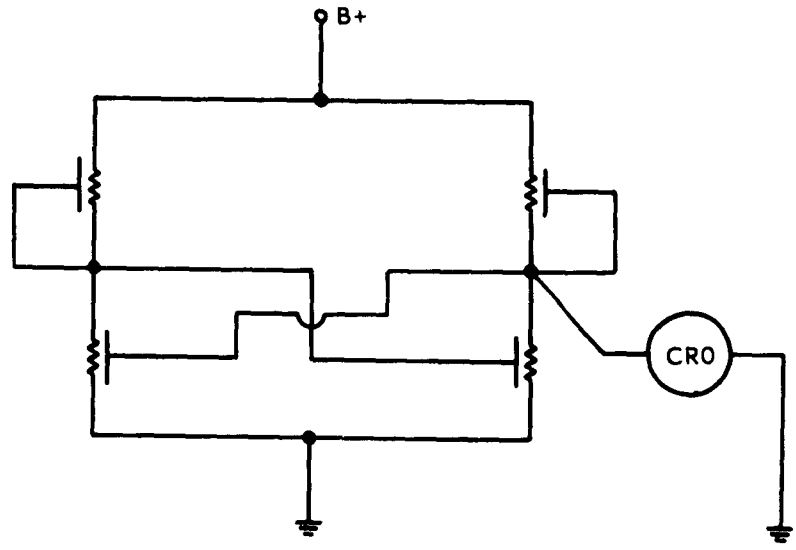


Figure 10. (a) Oscillator Schematic Diagram and (b) Output Voltage Waveform



10V/cm
RISE TIME ≈ 200μ SEC
FALL TIME ≈ 250μSEC

Figure 11. (a) Multivibrator Schematic Diagram and (b) Output Voltage Waveform

Work has been directed toward obtaining an alloy-diffused transistor. One mil diameter dots of In-1% Al-1.5% As have been alloyed into 1 ohm-cm silicon slices. After solvent removal, the slices were diffused for one hour at 1100°C. Measurements of collector-to-emitter breakdown voltage with open base contact (BV_{ceo}) have indicated very narrow base widths. Because of excessive current heating resulting from avalanche breakdown, the units were easily destroyed. These and other preliminary results have demonstrated that considerable technology remains to be developed. In addition, some effort has been directed toward the formation of doubly diffused structures.

Because of the success in forming active elements and, especially, active junction devices which can be completely deposited, the temperature and radiation characteristics have been reviewed. First, it is obvious that, from the standpoint of radiation resistance, deposited crystallite junction devices offer no advantages over bulk junction devices. Second, it has been concluded from the earlier study that GaP and SiC are the materials which are technologically the most advanced for junction device operation at 500°C. GaAs is probably limited to 300-400°C operation. To obtain single crystals by direct deposition, a material must be deposited onto a substrate that is about the crystal "epitaxial" temperature. For GaP, this temperature is 1100°C and, for SiC, it is 2000°C. Clearly, substrate and vapor pressure requirements are severe for these materials, and it is concluded that high-temperature devices will be quite difficult to deposit directly. Because of this conclusion and the greater promise of the thin-film field effect and barrier devices, it is planned to carry on only a low level effort directed toward development of point contacts in SiC.

It is a matter of interest to summarize the deposited transistor work so far and to put the effort in perspective, as in figure 12. It is seen from the illustration that all-deposited diodes and active devices were formed in crystallites. Silicon crystallites of up to 10-20 mils in size have been obtained in this program. Three approaches to transistor formation were pursued with the following results: (a) material deposition techniques have been developed, (b) materials have been improved, (c) evaluation techniques for micro-crystals were developed, (d) all-deposited junction devices have been built, (e) active junction devices have been developed, and (f) a variety of specialized microdevice techniques have been developed. Although this work is now being deemphasized, the techniques and devices resulting from it will have wide applicability for other aspects of the program.

Some equipment that was recently assembled for device work is shown in three photographs. Figure 13 shows resistivity test equipment used for material evaluation. Figure 14 is a photograph of a thermal compression bonder, assembled from basic Kulicke and Soffa Mfg. Co. parts, and a 3-point device probe is shown in figure 15.

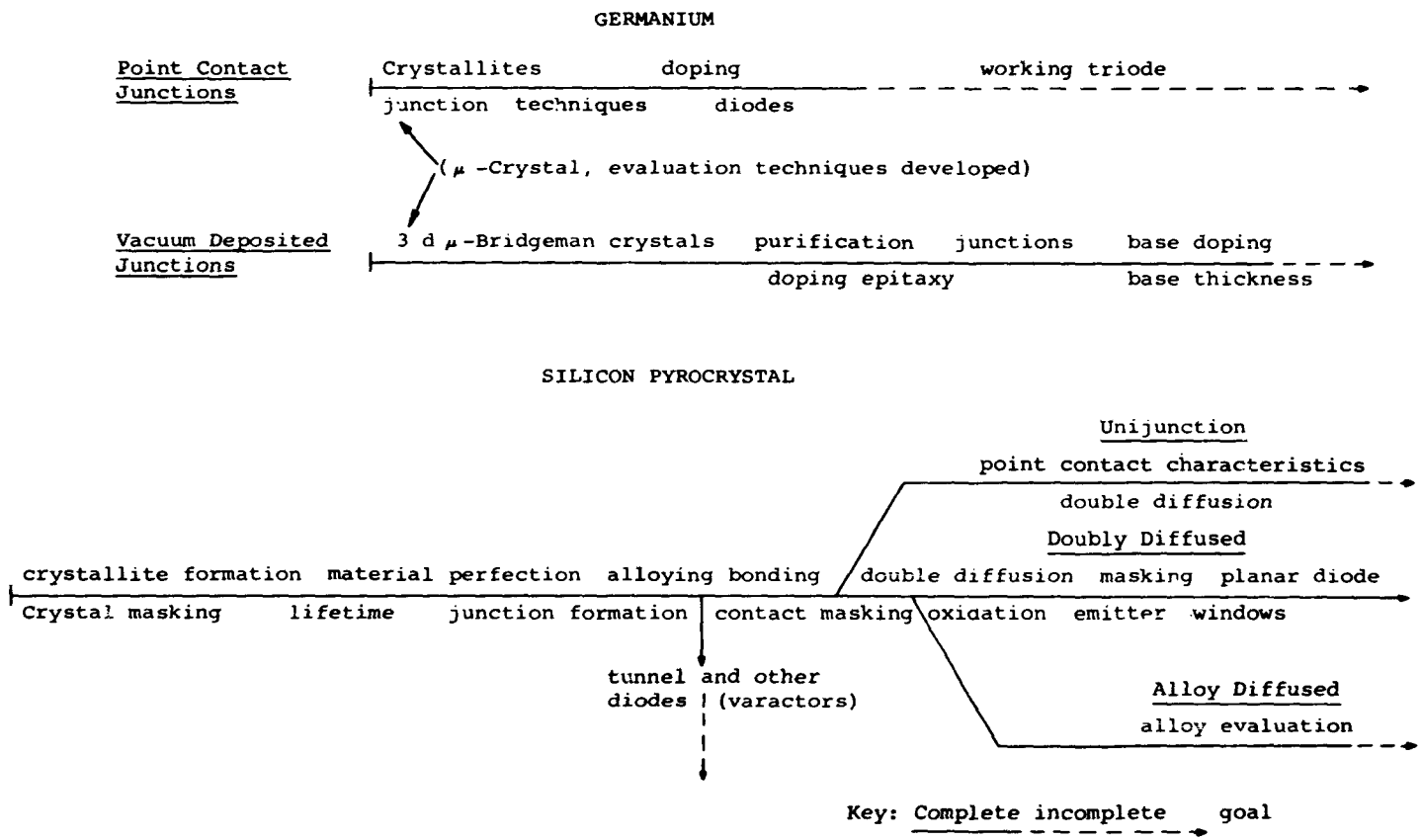


Figure 12. Status of Evaporated Junction Transistors

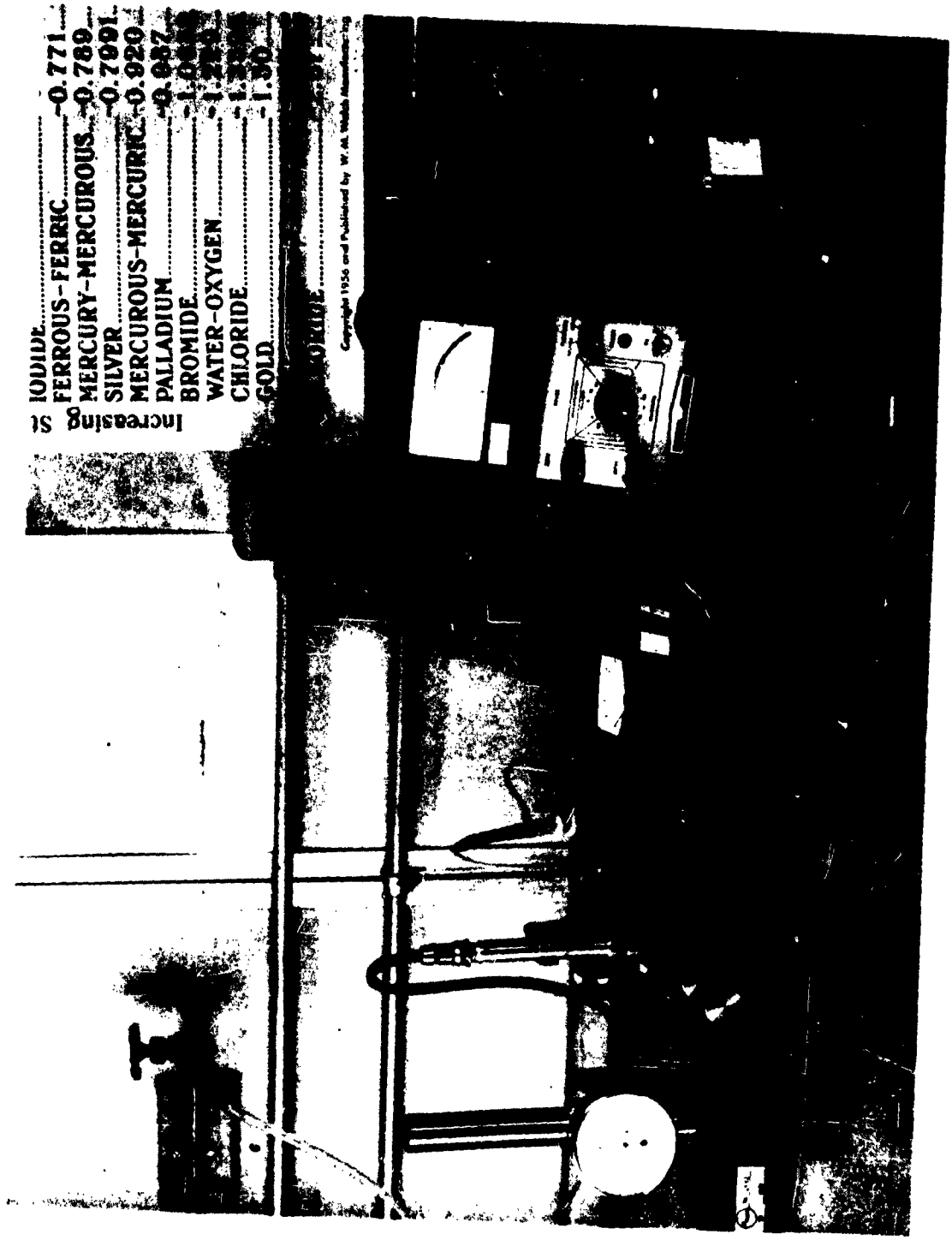


Figure 13. Thickness Gauge and Resistivity Test Set

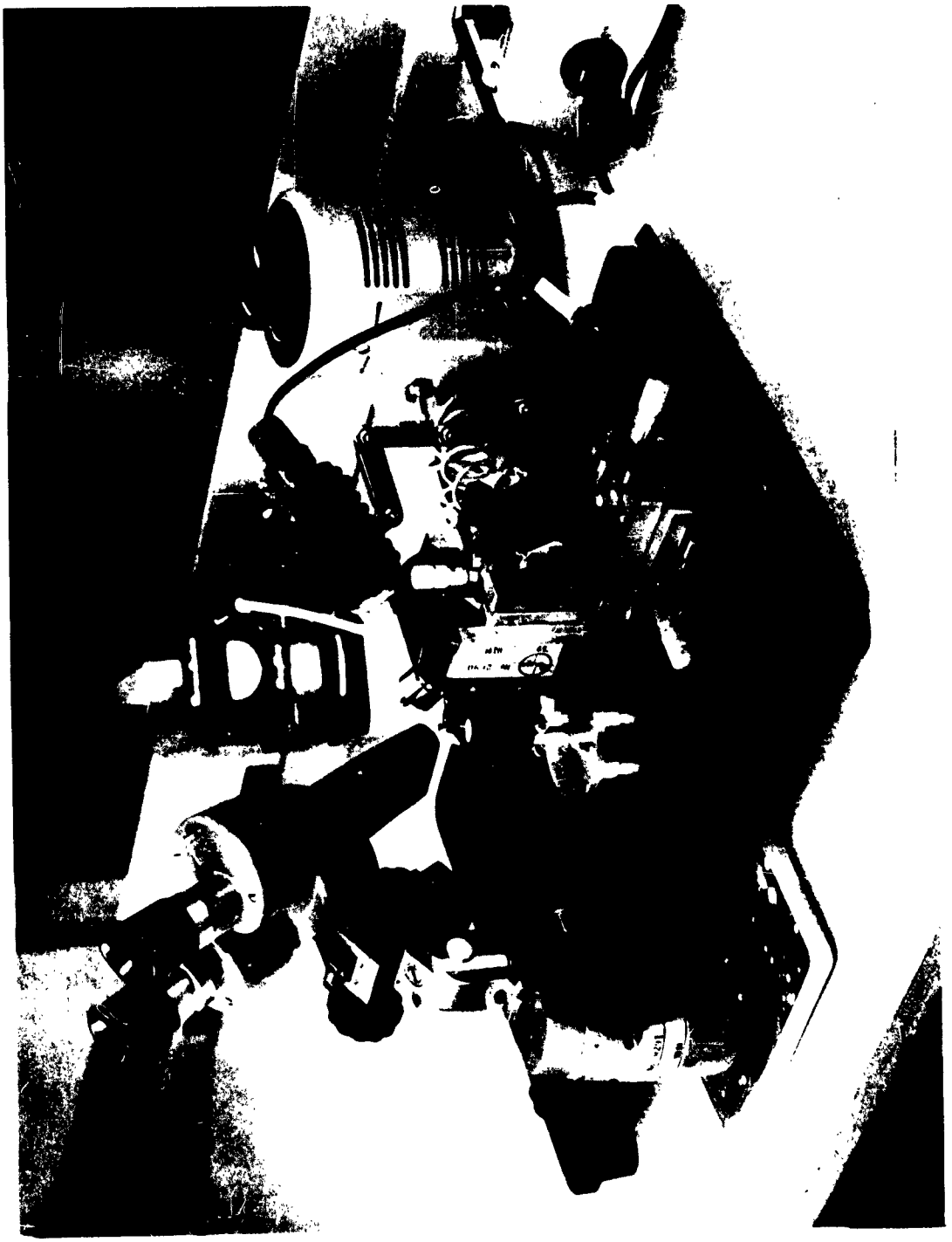


Figure 14. Thermal Compression Border

Figure 15. Three-point Probe Micromanipulator

4. CONCLUSION

The work, in general, has been proceeding according to schedule. The lack of high-temperature dielectric materials is not delaying the program. The present dielectric materials, which are capable of going to over 400°C, are sufficient for the studies currently being performed. The study of the refractory oxides, such as neodymium and hafnium will hopefully lead to dielectrics that will operate to 500°C. These dielectrics are needed not only for capacitors but, for insulators in field effect devices, resistors and other circuit functions.

The studies of field effect phenomena have proved singularly successful. Since the beginning of our study, first reported in the fourth quarterly report, numerous other laboratories have taken up this work with equal success. This is, of course, in keeping with our ultimate objective "of providing instruction for the formation of complete thin film circuits." Because most semiconductors exhibit field effect, to some extent, the chief research that must be performed is that of determining the proper materials that will enable the device to operate to 500°C. Exploratory work was carried out this quarter on circuits utilizing field effect devices. It is now believed that, with proper improvements, field effect devices will be useful for many general circuit applications.

Because of the requirements for high temperature, emphasis on both sputtering and pyrolytic film formation is being placed currently on silicon carbide. When films of this material are satisfactorily formed, they will be examined for field effects, junction effects, and other pertinent parameters to evaluate their potential in thin-film circuitry.

Senior personnel now participating in work on this contract are:

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Mr. Ernest G. Bylander
Dr. Charles Feldman
Mr. Charles Gane
Mr. Michael Hacskaylo
Mr. Wilbur T. Layton
Dr. Maurice M. Mitchell, Jr.
Dr. Charles W. Moulton
Mr. Herbert L. Wilson

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